REMARKS

Claims 1-20 are pending in this application. By this Amendment, claims 1, 17 and 19 are amended. Reconsideration based on the above amendments and following remarks is respectfully requested.

I. The Claims Define Allowable Subject Matter

The Office Action rejects claims 1, 2, 4-6, 8-10 and 19 under 35 U.S.C. §102(e) as being unpatentable in view of U.S. Patent No. 6,407,728 to Sekine; claims 16-18 and 20 under 35 U.S.C. §102(b) as being unpatentable in view of U.S. Patent No. 5,764,210 to Moon; and claims 3, 7 and 11-15 under 35 U.S.C. §103(a) as being unpatentable over Sekine. These rejections are respectfully traversed.

With respect to claims 1-15 and 17-19, Sekine fails to disclose an input terminal that receives a display signal including a predetermined signal used for generating a common signal and multiple pixel signals to be supplied to the multiple pixels, wherein the predetermined signal is embedded into a predetermined period between a group of pixel signals and another group of pixel signals in the display signal, as recited in claim 1, and similarly recited in claims 17 and 19.

Instead, Sekine discloses the sample hold circuit 111 is provided for sampling and holding image signals for one horizontal time period (col. 9, lines 63-65; Fig. 3). To be more specific, the sample hold circuit 111 samples and holds multiple pixel signals included in a display signal for one horizontal time period, one by one, and the multiple pixel signals are then output separately from respective output terminals of the sample hold circuit 111. Thus, for a certain horizontal time period, each of the different pixel signals is output from each of the output terminals of the sample hold circuit 111. Because of this arrangement, with respect to plural horizontal time periods, as shown by D1 in Fig. 4, one pixel signal is sequentially

output per one horizontal time period (Th period) from each of the output terminals of the sample hold circuit 111.

Moreover, Sekine discloses that in the first half period "Tdat" of one horizontal time period (Th period), each of the first switches 112 switches to connect the fixing terminal and the output terminal of the sample hold circuit 111 (the second switching terminal "B"), and in the second half period "Tcom", each of the first switches 112 switches to connect the fixing terminal to a single panel-common line "Com" (the first switching terminal "A") (col. 11, line 66 - col. 12, line 24; Fig. 3). As shown by C1 in Fig. 4, a common voltage signal is applied to the single panel-common line "Com" (Fig. 4). With respect to a certain horizontal time period, the fixing terminal of the first switches 112 outputs a pixel signal to amplifiers 113 in the first half period "Tdat", and in the second half period "Tcom", a common voltage signal is output to the amplifiers 113. As such, with respect to a plurality of horizontal time periods, a pixel signal and a common voltage signal are alternately input to the amplifiers 113 from the fixing terminal of the switches 112. Thus, a common voltage signal is put between a pixel signal and another pixel signal.

In contrast, in the claimed invention, a predetermined signal for generating a common signal, which is included in a display signal that is input to an input terminal of a liquid crystal device, is embedded between a group of pixel signals and another group of pixel signals. The claimed invention is, therefore, distinguishable from Sekine who puts a common voltage signal between a pixel signal and another pixel signal.

Thus, Sekine fails to disclose all of the features of claims 1, 17 and 19. As such, it is respectfully submitted, that claims 1, 17 and 19 are distinguishable over the applied art. Furthermore, claims 2-15, which depend from claim 1, and claim 18, which depends from claim 17, are likewise distinguishable over the applied art for at least the reasons discussed

above, as well as for the additional features they recite. Accordingly, withdrawal of the rejection under §§102 and 103 is respectfully requested.

With respect to the rejection of claims 16-18 and 20, Moon fails to disclose a display signal generation circuit that combines the multiple pixel signals with a predetermined signal, which is used for generating a common signal as recited in claim 16, and similarly recited in claims 17 and 20.

Instead, Moon discloses a video signal input to common electrode correcting circuit 15 is integrated by integrator 17 and held by sampling/holding portion 18 (col. 4, lines 37-49). Gain controller 19 controls the voltage of the data waveform of sampling/holding portion 18, and the controlled voltage waveform is added to the common electrode signal, generating a corrected common electrode signal (col. 4, lines 49-52).

In Moon, a display signal is not combined with a predetermined signal, which is used for generating a common signal, but instead the display signal is integrated, sampled and held. Furthermore, as discussed above, the voltage waveform obtained through gain controlling is only added to the common electrode signal.

However, such a voltage waveform obtained from a display signal, is different from the display signal itself. Thus, Moon fails to disclose all of the features of claims 16, 17 and 20. As such, it is respectfully submitted, claims 16, 17 and 20 are distinguishable over the applied art. Furthermore, claim 18, which depends from claim 17, is likewise distinguishable over the applied art for at least the reasons discussed above, as well as for the additional features it recites. Accordingly, withdrawal of the rejection under §102 is respectfully requested.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

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